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10/816,391	03/31/2004	Mikhail Dorojevets	SONY-27300	1665

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Jonathan O. Owens
HAVERSTOCK & OWENS LLP
162 North Wolfe Road
Sunnyvale, CA 94086

EXAMINER	
HOLDER, ANNER N	

ART UNIT	PAPER NUMBER
2621	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,391	DOROJEVETS ET AL.	
	Examiner	Art Unit	
	ANNER HOLDER	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/09/08*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48,50 and 51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48,50 and 51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 09/09/08 have been fully considered but they are not persuasive. As to Applicant's arguments regarding reference Heaton lacking teaching of a global accumulation unit to accumulate the results of the processing operations for each processing element, Examiner respectfully disagrees and maintains position regarding Applicant's argument. Heaton teaches local accumulation thus it would have been obvious and is fairly suggested by the reference to store results for each processing element in one central location (global accumulation). [Fig. 6; Pg. 367 Col. 2 ¶ 1 (sum or tree); pg 364 I. Introduction]

2. Applicant's arguments see page 3 Objections to the Claims, filed 09/09/08, with respect to claim 41 have been fully considered and are persuasive. The objection of claim 41 has been withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 7, 8, 11, 13-16, 41, 44 and 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990.

5. As to claim 1, Heaton teaches a video processing apparatus comprising: a. a memory; [Pg. 365 Col. 2 ¶ 1] and b. one or more video processing modules, each video processing module coupled to the memory and comprising: i. a programmable array of processing elements, each processing element including local registers to provide data used in processing operations and to store results of the processing operations; [Pg. 364 I Introduction; Pg. 364 Col. 2 ¶ 1 – Pg. 366 Col. ¶ 1] ii. a block load and store unit coupled to the programmable array of processing elements to load, store, and send data transferred back and forth between the memory and the array of processing elements; [Pg. 365 Col. 1 ¶ 1 – Pg. 366; Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1 - Col. 2 ¶ 1] iii. a global accumulation unit to accumulate the results of the processing operations for each processing element [Fig. 6; Pg. 367 Col. 2 ¶ 1 (sum or tree)] and iv. a local controller to provide instructions and parameters related to the processing operations and data transfer. [Fig. 7; Pg. 364-365 II Blitzen Chip Architecture]

Heaton teaches local accumulation thus it would have been obvious and is fairly suggested by the reference to store results for each processing element in one central location (global accumulation). [Fig. 6; Pg. 367 Col. 2 ¶ 1 (sum or tree); pg 364 I. Introduction]

6. As to claim 2, Heaton teaches the array of processing elements comprises a two-dimensional array. [Fig. 5; Col. 1 ¶ 1 - Col. 2]

7. As to claim 7, Heaton teaches the block load and store unit comprises one or more arrays of exchange registers. [Pg. 365-366 Col. 2 ¶ 1; Fig. 6]

8. As to claim 8, Heaton (modified by Taylor) teaches each array of exchange registers is a two-dimensional array. [Fig. 6 (N Bit Shift Register)]

9. As to claim 11, Heaton teaches a direct, high-bandwidth data path to couple each of the video processing modules to the memory. [Pg. 365 Col. 2 ¶ 1]

10. As to claim 13 Heaton teaches the block load and store unit sends data transferred back and forth between non-adjacent processing elements of the array of processing elements. [Fig. 5; Pg. 365-366 ¶ 1]

11. As to claim 14, Heaton teaches each processing element includes a local accumulation register. [Fig. 6; PG. 366 III Blitzen PE Architecture ¶ 1-3]

12. As to claim 16, Heaton teaches the block load and store unit sends data transferred back and forth between the local registers in the processing elements, the global accumulation unit, and the local controller. [Fig. 6; Pg. 366 Pg. 366 III Blitzen PE Architecture]

13. As to claim 41, Heaton teaches a programmable array of processing elements to process video, each processing element including local registers to store video data blocks received from a main memory, to process the received video data blocks, and to store results of processing the video data blocks, [Fig. 6; Pg. 365 Col. 2 ¶ 1 -Pg. 366 Col. 1 ¶ 2] wherein each processing element is configured to send the results to a global accumulation unit to accumulate the results of the processing operations for each processing element. [Fig. 6; Pg. 367 Col. 2 ¶ 1 (sum or tree)]

14. As to claim 44, Heaton teaches the array of processing elements comprises a two-dimensional array. [Fig. 5; Col. 1 ¶ 1 - Col. 2]

15. As to claim 50, Heaton each processing element includes a local accumulation register. [Fig. 6; PG. 366 III Blitzen PE Architecture ¶ 1-3]

16. As to claim 51, Heaton each processing element further comprises a plurality of control registers including a PE mask register, a condition register, a block base register, and a vector base register. [Fig. 6; Pg. 366 III Blitzen PE Architecture]

17. Claims 3-4, 9-10, 42-43 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Taylor US 4,992,933.

18. As to claim 3, Heaton teaches the limitations of claim 2.

Heaton does not specifically teach the two-dimensional array comprises a 4X4 ray of processing elements.

Taylor teaches the two-dimensional array comprises a 4X4 ray of processing elements. [Col. 3 Lines 60-67]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, providing array processing elements a greater degree of flexibility. [Taylor Col. 1 Lines 64-66]

19. As to claim 4, Heaton teaches the limitations of claim 2.

Heaton does not specifically the two-dimensional array comprises a single-instruction multiple-data array.

Taylor teaches the two-dimensional array comprises a single-instruction multiple-data array. [Taylor - Abstract; Col. 1 Lines 8-10; Col. 2 Lines 3-12; Col. 31-35]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, providing a SIMD array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66]

20. As to claim 9, Heaton teaches the limitations of claim 1.

Heaton does not specifically teach local controller provides control commands to each processing element, performing control and processing operations on data stored within the local controller, and transfers data between the local controller and other registers within one video module.

Taylor teaches the local controller provides control commands to each processing element, performing control and processing operations on data stored within the local controller, and transfers data between the local controller and other registers within one video module. [Taylor – Fig. 1; Col. 3 Lines 31-39; Col. 4 Lines 7-58; Fig. 2; Fig. 4; Fig. 8]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, allowing for communication and global control of processing elements with in the array.

21. As to claim 10, Heaton (modified by Taylor) teaches a system controller coupled to the memory and to the one or more video processing modules. [Taylor – Fig. 1; Col. 4 Lines 7-58]

22. As to claim 42, Heaton teaches the limitations of claim 41.

Heaton does not specifically teach processing elements coupled to a local controller to provide instructions and parameters related to data transfer and processing of the video data blocks received from the main memory.

Taylor teaches processing elements coupled to a local controller to provide instructions and parameters related to data transfer and processing of the video data blocks received from the main memory. [Abstract; Col. 3 Lines 31-59]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, allowing for communication and global control of processing elements with in the array.

23. As to claim 43, Heaton (modified by Taylor) teaches the limitations of claim the local controller provides control commands to each processing element, performing control and processing operations on data stored within the local controller, and transfers data between the local controller and other registers within one video module. [Taylor – Fig. 1; Col. 3 Lines 31-39; Col. 4 Lines 7-58; Fig. 2; Fig. 4; Fig. 8]

Heaton does not specifically teach processing elements coupled to a local controller to provide instructions and parameters related to data transfer and processing of the video data blocks received from the main memory.

Taylor teaches processing elements coupled to a local controller to provide instructions and parameters related to data transfer and processing of the video data blocks received from the main memory. [Abstract; Col. 3 Lines 31-59]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, providing a SIMD array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66]

24. As to claim 45, Heaton teaches the limitations of claim 44.

Heaton does not specifically teach the two-dimensional array comprises a 4X4 ray of processing elements.

Taylor teaches the two-dimensional array comprises a 4X4 ray of processing elements. [Col. 3 Lines 60-67]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, providing array processing elements a greater degree of flexibility. [Taylor Col. 1 Lines 64-66]

25. As to claim 46, Heaton teaches the limitations of claim 2.

Heaton does not specifically the two-dimensional array comprises a single-instruction multiple-data array.

Taylor teaches the two-dimensional array comprises a single-instruction multiple-data array. [Taylor - Abstract; Col. 1 Lines 8-10; Col. 2 Lines 3-12; Col. 31-35]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, providing a

SIMD array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66]

26. Claims 12 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Buchholz et al. (Buchholz) US 4,745,547.

27. As to claim 12, Heaton teaches the limitations of claim 1.

Heaton does not specifically teach each processing element further comprises a plurality of scalar registers.

Buchholz teaches a plurality of scalar registers. [Col. 6 Lines 5-8]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Buchholz with the device of Heaton allowing improvements to image processing.

28. As to claim 49, see the rejection of 12.

29. Claims 5-6, 15 and 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Agarwal et al. (Agarwal) US 5,680,338.

30. As to claim 5, Heaton teaches each processing element includes a plurality of block registers. [Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2 (memory registers)]

Heaton does not specifically teach vector registers.

Agarwal teaches vector registers. [Figs. 2-4; Col. 6 Lines 16-33, 57-65]

It would have been obvious to one of ordinary skill in the art to incorporate the teachings of Agarwal in the device of Heaton, allowing for improvements in image processing and image quality.

31. As to claim 6, Heaton (modified by Agarwal) teaches each block register is configured to hold 8 8-bit data elements as a two-dimensional 2X4 block of pixels or 4 16-bit data elements as a one-dimensional vector. [Agarwal - Figs. 2-4; Col. 6 Lines 16-33, 57-65]

32. As to claim 15, Heaton (modified by Agarwal) teaches each processing element further comprises a plurality of control registers including a PE mask register, a condition register, a block base register, and a vector base register. [Heaton - Fig. 6; Pg. 366 III Blitzen PE Architecture; Agarwal - Figs. 2-4; Col. 6 Lines 16-33, 57-65]

33. As to claim 47, Heaton (modified by Agarwal) teaches each processing element includes a plurality of vector registers and a plurality of block registers. . [Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2 (memory registers)]

Heaton does not specifically teach vector registers.

Agarwal teaches vector registers. [Figs. 2-4; Col. 6 Lines 16-33, 57-65]

It would have been obvious to one of ordinary skill in the art to incorporate the teachings of Agarwal in the device of Heaton, allowing for improvements in image processing and image quality.

34. As to claim 48, Heaton (modified by Agarwal) teaches each vector register and each block register is configured to hold 8 8-bit data elements as a two-dimensional

2.times.4 block of pixels or 4 16-bit data elements as a one-dimensional vector. [Agarwal - Figs. 2-4; Col. 6 Lines 16-33, 57-65]

35. Claims 17-26, 28, 29-38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Taylor US 4,992,933 further in view of Agarwal et al. (Agarwal) US 5,680,338.

36. As to claim 17, Heaton teaches a method of processing video comprising: a. configuring a video stream into data blocks; [Fig. 3; Pg. 365-366 Col. 1 ¶ 1] b. loading data blocks from memory to a first array of exchange registers; [Fig. 6 (shift registers)] c. loading data blocks from the first array of exchange registers to a programmable array of processing elements, wherein each processing element within the array of processing elements includes an array of block registers, an array of vector registers, and a local accumulator, the data blocks are loaded from the first array of exchange registers to the array of block registers; [Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1 – Col. 2 ¶ 1] e. processing the data blocks loaded in the array of vector registers and storing results in the corresponding local accumulator for each processing element; [Fig. 6; Pg. 365-366] f. accumulating the results stored in the local accumulators in a global accumulator, thereby forming accumulated results. [Fig. 6; Pg. 367 Col. 2 ¶ 1 (sum or tree)]

Heaton does not specifically teach moving the results into a local controller.

Taylor teaches moving the results into a local controller. [Abstract; Fig. 1; Col. 5 Lines 22-28]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, providing array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66]

Heaton (Modified Taylor) does not specifically teach loading the data blocks from the array of block registers to the array of vector registers.

Agarwal teaches loading the data blocks from the array of block registers to the array of vector registers. [Col. 4 Lines 37-49; Col. 5 Lines 45-59; Figs. 2-4; Col. 6 Lines 16-33, 57-65]

It would have been obvious to one of ordinary skill in the art to incorporate the teachings of Agarwal in the device of Heaton modified by Taylor, allowing for improvements in image processing and image quality.

37. As to claim 18, Heaton (modified by Taylor and Agarwal) teaches storing results from processing the data blocks in the array of vector registers, and loading the results stored in the array of vector registers in the array of block registers. [Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2 (memory registers); Agarwal - Col. 4 Lines 37-49; Col. 5 Lines 45-59; Figs. 2-4; Col. 6 Lines 16-33, 57-65]

38. As to claim 19, Heaton (modified by Taylor and Agarwal) teaches loading the results in the array of block registers into a second array of exchange registers, and loading the results from the array of block registers into memory. [Taylor – Fig.1; Fig. 2; Col. 5 Lines 18-28; Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2]

39. As to claim 20, Heaton (modified by Taylor and Agarwal) teaches each of the first and second array of exchange registers is a two-dimensional array. [Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2; Fig. 5; Pg. 365-366 Col. 2 ¶ 1]

40. As to claim 21, Heaton (modified by Taylor and Agarwal) teaches loading the results in the array of block registers into a second array of exchange registers, and loading the results in the second array of exchange registers into another array of block registers included within non-adjacent processing elements to the processing elements including the array of block registers. [Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2; Fig. 5; Pg. 365-366 Col. 2 ¶ 1]

41. As to claim 22, Heaton (modified by Taylor and Agarwal) teaches loading the results in the array of block registers into another array of block registers included within a processing element adjacent to the processing element including the array of block registers. Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2; Fig. 5; Pg. 365-366 Col. 2 ¶ 1]

42. As to claim 23, Heaton (modified by Taylor and Agarwal) teaches the array of processing elements comprises a two-dimensional array. [Heaton - Fig. 5; Col. 1 ¶ 1 - Col. 2]

43. As to claim 24, Heaton (modified by Taylor and Agarwal) teaches the two-dimensional array comprises a 4X4 array of processing elements. [Taylor - Col. 3 Lines 60-67]

44. As to claim 25, Heaton (modified by Taylor and Agarwal) teaches the two-dimensional array comprises a single-instruction multiple-data array. [Agarwal - Figs. 2-4; Col. 6 Lines 16-33, 57-65]

45. As to claim 26, Heaton (modified by Taylor and Agarwal) teaches each vector register and each block register is configured to hold 8 8-bit data elements as a two-dimensional 2X4 block of pixels or 4 16-bit data elements as a one-dimensional vector. [Agarwal - Figs. 2-4; Col. 6 Lines 16-33, 57-65]

46. As to claim 28, Heaton (modified by Taylor and Agarwal) teaches the local controller utilizes the accumulated results to make control decisions related to video processing. [Taylor – Abstract; Col. 3 Lines 31-59; Heaton - Pg. 367 Col. 2 ¶ 1]

47. As to claim 29, see rejection of claim 17 above.

48. As to claim 30, see rejection of claim 18 above.

49. As to claim 31, see rejection of claim 19 above.

50. As to claim 32, see the rejection of claim 20 above.

51. As to claim 33, see rejection of claim 21 above.

52. As to claim 34, see rejection of claim 22 above.

53. As to claim 35, see rejection of claim 23 above.

54. As to claim 36, see rejection of claim 24 above.

55. As to claim 37, see rejection of claim 25 above.

56. As to claim 38, see rejection of claim 26 above.

57. As to claim 40, see rejection of claim 28 above.

58. Claim 27 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Taylor US 4,992,933 in view of Agarwal et al. (Agarwal) US 5,680,338 further in view Buchholz et al. (Buchholz) US 4,745,547.

59. As to claim 27, Heaton teaches that processing the data blocks includes processing data blocks loaded from the array of block registers and data loaded from the array of scalar registers. [Fig. 5; Pg. 365 Col. 1 ¶ 1 – Pg. 366; Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1 - Col. 2 ¶ 1; teaches the loading and transfer from elements including registers)]

Heaton does not specifically teach each processing element further comprises a plurality of scalar registers.

Buchholz teaches a plurality of scalar registers. [Col. 6 Lines 5-8]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Buchholz with the device of Heaton allowing improvements to image processing.

60. As to claim 39, see rejection of claim 27 above.

Conclusion

61. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

62. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANNER HOLDER whose telephone number is (571)270-1549. The examiner can normally be reached on M-Th, M-F 8 am - 3 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anner Holder/
Examiner, Art Unit 2621 12/04/08
/Tung Vo/
Primary Examiner, Art Unit 2621